GigE Vision Cores Family Design Note

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Terms and Abbreviations

AOI	Area of Interest.
DDR	Double Data Rate interface. Signals of this interface might change its state on both rising and falling edges of a clock.
EPC	External Peripheral Controller core from Xilinx Platform Studio. It provides synchronous interface to connect custom peripherals to the CPU system bus.
GVCP	GigE Vision Control Protocol. See the GigE Vision Specification for details.
GVSP	GigE Vision Streaming Protocol. See the GigE Vision Specification for details.
SDR	Single Data Rate interface. Signals of this interface may change its state either on rising or on falling edge of a clock but not on both.
SHA	Secure Hash Algorithm.
SDRAM	In this document it always means SDR Synchronous Dynamic RAM unless there is explicitly stated DDR or DDR2.
XST	Xilinx Synthesis Technology. The FPGA synthesis tool provided by Xilinx, Inc.

Overview

The family of the GigE Vision IP cores allow system integrator to build a GigE Vision compliant device with minimum effort. The cores implement the GigE Vision functionality and user can concentrate on a device-specific features only.

The set of cores require some particular external components for their proper operation. This design note discusses these additional required components.

Sample GigE Vision System

Figure 1 shows block diagram of a sample system build of the GigE Vision cores and some additional modules. The digram shows connection of the required external components.

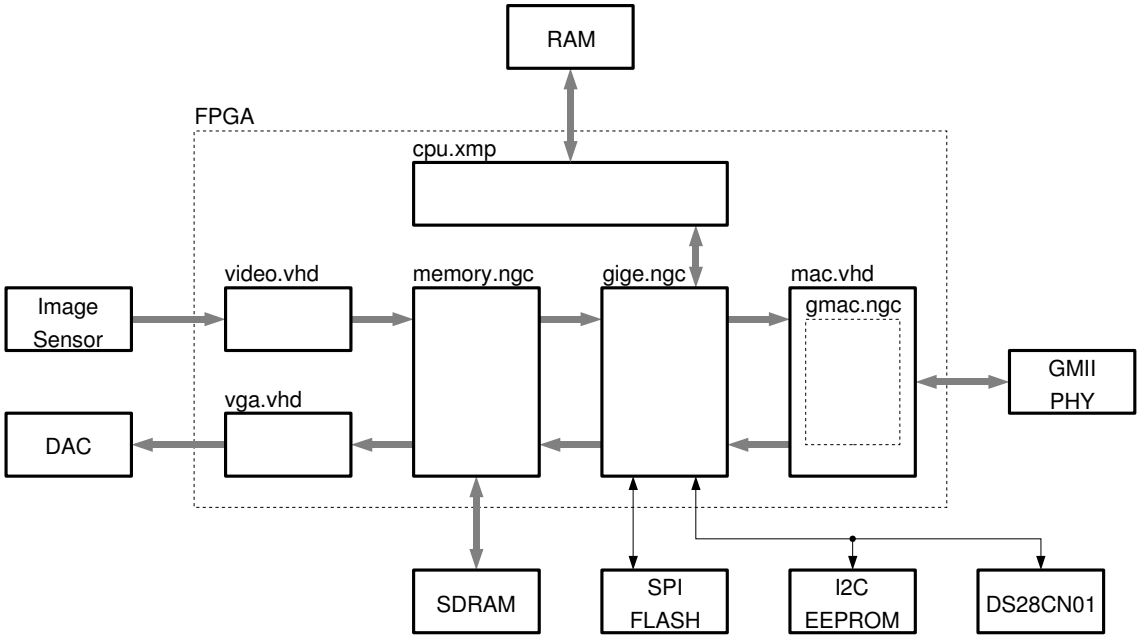

Figure 1: Block diagram of a system based on the set of GigE Vision cores

The block digram shows extended system using advanced features of the cores that extend functionality over the scope of the GigE Vision Specification. Typical GigE Vision device does not use the data stream receiver functionality.

External Components

As mentioned above, the cores require particular external components for their proper operation. These components comprehend mainly various memories.

Components Description

SDRAM

The SDRAM is used as an image framebuffer. The standard space-saving framebuffer design operates with 16-bits wide SDRAM device with capacity of 8 or 32 MB.

There exists extended version of the framebuffer in form of custom personality interface module for the Xilinx Multi-Port Memory Controller. This variant is discussed below in dedicated chapter.

SPI FLASH

The SPI flash memory is used to store FPGA bitstream, CPU firmware, and device description XML file. By default, 64 Mb memory is used. Required minimum is 32 Mb. Tested and recommended are Intel S33 and STMicroelectronics M25P serial flash memories.

I^2C EEPROM

The I^2C serial EEPROM is required for non-volatile storage of parameters what is required by the GigE Vision Specification. The core expects at least 64 kb EEPROM to be attached. As the core generates 16-bit address, it is possible to use EEPROMs with densities from 64 to 512 kb. Tested and recommended device is M24C64.

DS28CN01

The DS28CN01 device from Maxim is an I^2C EEPROM with integrated SHA-1 engine. It is used for authentication and unlocking the IP cores.

CPU RAM

The CPU requires at least 256 kB of the external RAM for its operation. Whole CPU subsystem is typically built in the Xilinx Platform Studio. This means that any external RAM devices supported by a XPS might be used. In the reference design there is simple 8-bits wide 4 MB SDRAM device used because it consumes less FPGA resources compared to faster DDR/DDR2 memory controllers.

It is possible to use the Xilinx Multi-Port Memory Controller for the CPU RAM and to share this memory controller with the image framebuffer. This option is discussed below.

GMII PHY

The MAC provides interface between FPGA and physical Ethernet link. The reference design as well as our standard products expect the PHY to be connected using the Gigabit Media-Independent Interface (GMII). Almost every available 1000BASE-T PHY supports this interface. The difference in the PHY devices available on the market is in a way of accessing their extended configuration and status registers. Fully tested and recommended PHY device is Broadcom BCM5461.

Summary

Requirements to the external components are summarized in Table 1. The components used in a custom design should be fully compatible except the CPU RAM.

Component	Characteristics	Recommended Device(s)
SDRAM	64Mb SDRAM, 16-bit data bus Configuration 1M × 16 × 4 banks CL2 at 100MHz	Micron MT48LC4M16A2-7E Samsung K4S641632H-TC60
SPI FLASH	64Mb SPI FLASH At least 33MHz clock frequency	Intel QH25F640S33B8 STMicroelectronics M25P64V6P
I^2C EEPROM	64kb to 512kb I^2C EEPROM 400kHz clock frequency Maximum write time 10ms	STMicroelectronics 24C64
SHA	I^2C EEPROM with SHA-1 engine	Maxim DS28CN01
CPU RAM[1]	32Mb SDRAM, 8-bit data bus CL2 at 100MHz	Micron MT48LC4M16A2-7E Samsung K4S641632H-TC60
GMII PHY	1000BASE-T operation GMII interface	Broadcom BCM5461 National Semiconductor DP83865[2] Marvell M88E1111[3]

Table 1: Required external components

The components listed in Table 1 were fully tested in several designs based on the set of GigE Vision cores. Even though other components might work, they have not been evaluated.

1 The reference design uses 16-bit wide SDRAM with 8 data lines unconnected.

2 This PHY device was not tested as extensively as the Broadcom one. The GigE Vision Reference Design officially supports the BCM5461 device only.

3 Only GMII interface of this device was tested.

MPMC Option

The sample system present at Figure 1 is simplest to use and consumes the least amount of FPGA resources. However, it is possible to use the Xilinx Multi-Port Memory Controller (MPMC) to gain more versatility.

MPMC Based System

Figure 2 shows block diagram of a sample GigE Vision system built around the MPMC.

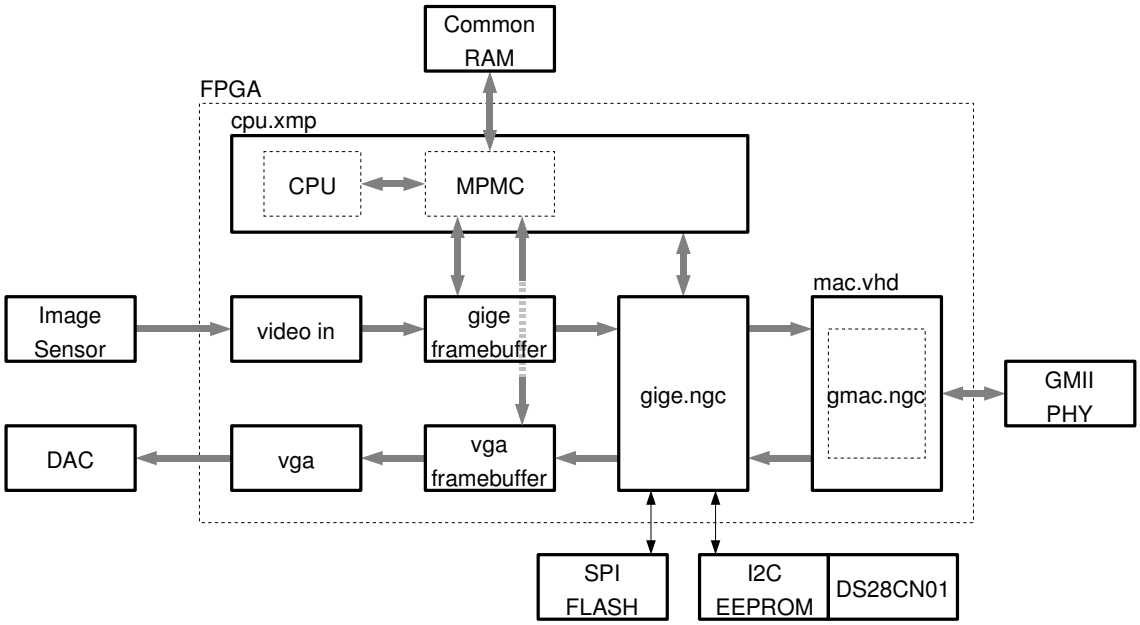

Figure 2: Block diagram of an MPMC based sample GigE Vision device

Compared to the system from Figure 1, the MPMC based system uses single common RAM subsystem. There are no separated memories for data path and CPU.

MPMC System Characteristics

The GigE Vision system differs from the simple reference design. Each of these two solutions have its own advantages and drawbacks. They are discussed below from the point of view of the MPMC based system.

Advantages

The MPMC based system has two main advantages over the solution with two dedicated RAMs:

- Single common memory for whole system – there is no need to place and route two memory devices on the PCB.
- Independence from the RAM technology – technology dependent part of the memory controller is implemented in the Xilinx MPMC. The framebuffer core remains the same for SDRAM/DDR/DDR2 chips/modules.

Drawbacks

Except the explicit advantages, the MPMC solution has even its own drawbacks:

- External memory data width – as the memory is shared by all system components, it has to provide sufficient bandwidth. The easiest way is to increase width of the external memory data bus to 32 or 64 bits.
- FPGA resources consumption – the MPMC itself consumes a lot of FPGA resources. Additionally, the MPMC has to be connected to a CPU using PLB bus. As a result, the minimal CPU system with OPB SDRAM controller and additional SDRAM framebuffer consumes less FPGA resources than similar CPU system with MPMC and the framebuffer personality interface module.

Revision History

Date	Version	Revision
2008-10-22	0.0.1	Initial draft of the document
2009-04-06	X-1.0	Final release of the Xilinx version
2009-05-26	X-1.0.1	Added the SHA-1 EEPROM external device
2009-12-02	X-1.0.2	Minor modifications regarding SPI flash and Ethernet PHY